CLAIMS:

1. A decoder circuit for a communication bus, the decoder circuit receiving a plurality of data signals from the communication bus, the data signals being susceptible of being received at different times, wherein the decoder circuit comprises:

- a correction circuit for correcting one or more of the input signals;
- a control signal for controlling the correction circuit;
- a gating circuit, the gating circuit arranged in the path of the control signal; and
- a gating control signal for controlling the gating circuit such that the control signal for controlling the correction circuit is blocked until a predetermined time.

2. A decoder circuit as claimed in claim 1, further comprising a parity circuit for generating a parity signal using the input data signals, the parity signal being used to generate said control signal for controlling the correction circuit.

3. A decoder circuit as claimed in claim 2, wherein the correction circuit comprises a plurality of multiplexers, each multiplexer receiving an input data signal, and a copy of the input data signal, from the communication bus;

- a comparison circuit for comparing the parity signal generated by the parity circuit with a parity signal received from the communication bus, the comparison circuit providing the control signal for controlling the plurality of multiplexers to output either the input data signal or the copy of the input data signal.

4. A decoder circuit as claimed in claim 3, wherein the gating circuit is located in the path of the control circuit such that it receives the output of the comparison circuit, and provides the control signal for controlling the plurality of multiplexers.

5. A decoder circuit as claimed in claim 2 or 3, further comprising a gating circuit provided in the path of each input data signal and each copy of the input data signal, and wherein the plurality of gating circuits are controlled by the gating control signal.

6. A decoder circuit as claimed in any one of claims 3 to 5, further comprising a gating circuit provided in the output path of each multiplexer, and wherein the plurality of gating circuits are controlled by the gating control signal.

7. A decoder as claimed in any one of claims 2 to 6, wherein the decoder is a dual-rail decoder.

8. A decoder circuit as claimed in claim 1, further comprising:

- a plurality of parity circuits, the parity circuits generating a plurality of parity signals from the input data signals;

means for generating a plurality of control signals using the parity signals, the control signals being used to control the correction circuit;

wherein a gating circuit is provided in the path between each parity signal and the means for generating the plurality of control signals.

9. A decoder circuit as claimed in claim 8, wherein the correction circuit comprises a plurality of XOR gates, each XOR gate receiving an input data signal from the communication bus, and a control signal from the means for generating control signals.

10. A decoder circuit as claimed in claim 9, wherein the means for generating control signals is a syndrome decoder.

11. A decoder circuit as claimed in any one of claims 8 to 10, wherein the decoder is a hamming decoder.

12. A decoder circuit as claimed in any one of the preceding claims, wherein the gating control signal is arranged to block the or each control signal from passing to the correction circuit until one or more of the input data signals have become stable.

13. A decoder circuit as claimed in any one claims 1 to 11, wherein the gating control signal is arranged to block the or each control signal from passing to the correction circuit until all of the input data signals have become stable.

14. A decoder circuit as claimed in any of one the preceding claims, wherein the gating control signal is a delayed version of a system clock signal.

15. A decoder circuit as claimed in any of claims 1 to 13, wherein the gating control signal is generated from the input data and/or parity bits.

16. A decoder circuit as claimed in any one of the preceding claims, wherein the gating circuit is an AND gate.

17. A decoder circuit as claimed in any one of claims 1 to 15, wherein the gating circuit is a latch.

18. A method of reducing power consumption in a decoder circuit for a communication bus, the decoder circuit receiving a plurality of data signals from the communication bus, the data signals being susceptible of being received at different times, wherein the decoder circuit comprises a correction circuit for correcting one or more of the input signals and a control signal for controlling the correction circuit,
wherein the method comprises the steps of providing a gating circuit in the path of the control signal, and controlling the gating circuit with a gating control signal, such that the control signal for controlling the correction circuit is blocked until a predetermined time.

19. A method as claimed in claim 18, wherein a parity circuit is provided for generating a parity signal using the input data signals, the parity signal being used to generate said control signal for controlling the correction circuit.

20. A method as claimed in claim 19, wherein the correction circuit comprises a plurality of multiplexers, each multiplexer receiving an input data signal, and a copy of the input data signal, from the communication bus, and a comparison circuit for comparing the parity signal generated by the parity circuit with a parity signal received from the communication bus, the comparison circuit providing the control signal for controlling the plurality of multiplexers to output either the input data signal or the copy of the input data signal.

21. A method as claimed in claim 20, further comprising the step of locating the gating circuit in the path of the control circuit such that it receives the output of the comparison circuit, and provides the control signal for controlling the plurality of multiplexers.

22. A method as claimed in claim 19 or 20, further comprising the step of providing a gating circuit in the path of each input data signal and each copy of the input data signal, and controlling the plurality of gating circuits with the gating control signal.

23. A method as claimed in any one of claims 20 to 22, further comprising the step of providing a gating circuit in the output path of each multiplexer, and controlling the plurality of gating circuits with the gating control signal.

24. A method as claimed in any one of claims 19 to 23, wherein the decoder is a dual-rail decoder.

25. A method as claimed in claim 18, further comprising the steps of:
providing a plurality of parity circuits, the parity circuits generating a plurality of parity signals from the input data signals;
providing means for generating a plurality of control signals using the parity signals, the control signals being used to control the correction circuit; and
providing a gating circuit in the path between each parity signal and the means for generating the plurality of control signals.

26. A method as claimed in claim 25, wherein the correction circuit comprises a plurality of XOR gates, each XOR gate receiving an input data signal from the communication bus, and a control signal from the means for generating control signals.

27. A method as claimed in claim 26, wherein the means for generating control signals is a syndrome decoder.

28. A method as claimed in any one of claims 25 to 27, wherein the decoder is a hamming decoder.

29. A method as claimed in any one of claims 18 to 28, wherein the gating control signal is arranged to block the or each control signal from passing to the correction circuit until one or more of the input data signals have become stable.

30. A method as claimed in any one claims 18 to 28, wherein the gating control signal is arranged to block the or each control signal from passing to the correction circuit until all of the input data signals have become stable.

31. A method as claimed in any one of claims 18 to 30, wherein the gating control signal is a delayed version of a system clock signal.

32. A method as claimed in any one of claims 18 to 30, wherein the gating control signal is generated from the input data and/or parity bits.

33. A method as claimed in any one of claims 18 to 32, wherein the gating circuit is an AND gate.

34. A method as claimed in any one of claims 18 to 32, wherein the gating circuit is a latch.